IPS Assemblers

Programmer's Reference

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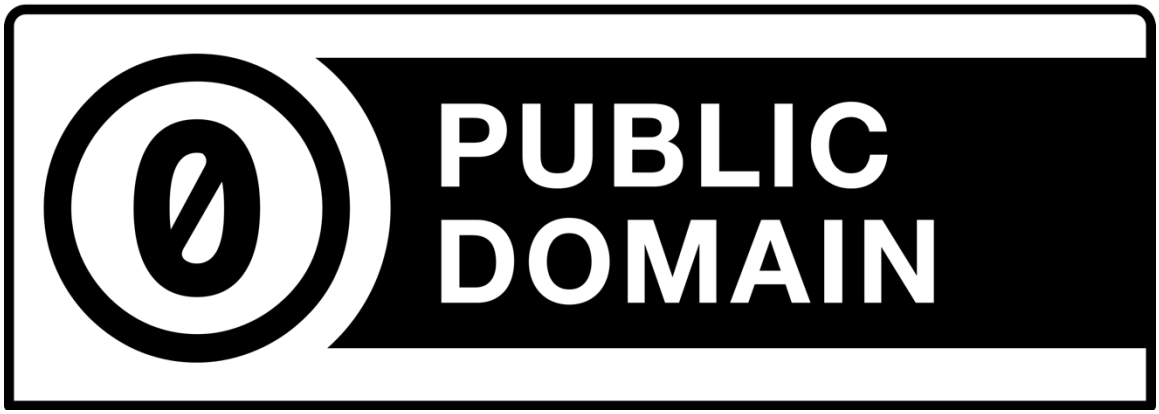

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IPS ASSEMBLERS

The following introduction to assembler programming in IPS explains the general principles involved. Briefly: DON'T. If you must, this introduction must be supplemented by the processor specific documentation for the processor that you will be using, and the machine specific documentation for the target that you will attempt to program on.

The principal reason for the development of the IPS assemblers is to allow the compilation of IPS for a particular target machine. (Normally this is a cross or X-Compilation)

Available assemblers

IPS assemblers have been written for the following processors:

- RCA 1802
- 6502
- 6800
- 6809
- 8080/Z80
- Am1601
- ARM

Use of assemblers in IPS

IPS has sufficient resources to program most problems without having to be intimately familiar with either the structure or the machine language of any particular target machine. The 3 major exceptions are:

i) to interface to particular hardware. The I/O structure of a particular IPS implementation may not be capable of the desired interface without modification, particularly if interrupts are involved.

ii) to program a time critical problem which can not be allowed any overhead. The IPS emulator has an overhead of typically 25 microseconds per executed word. Further, IPS treats all numbers as 16-bit. This results in an overhead if only bytes need to be manipulated. These two effects result in IPS programs typically running about 2 to 3 times slower than optimum machine code.

iii) to program special mathematical operations, such as rotational operations which would be inefficient using the standard IPS operators.

All these classes of problems are addressed by the ability to define new IPS words in terms of machine instructions rather than other IPS words. These newly defined words can then be used in the same fashion as other IPS words, but giving the programmer machine level access.

The IPS assembler provides the ability to define new words for a particular processor/machine. For the programmer to use an assembler successfully they must be familiar with the particular assembler that is used with their target machine.

Assembler applications

The IPS assemblers are intended mainly for short routines, that interface between high level IPS, the processor and application hardware. The IPS assemblers are not intended to support extended programs.

Assembly programs are hard to debug, often use more memory than the high-level equivalent, and are machine specific. Assembler routines cannot easily be transferred from one processor to another.

When programming time critical routines in assembler, it is usually only worthwhile assembly coding the inner loop.

Assemblers are for consenting adults (!) only

Assembler philosophy.

The assemblers have been kept as simple and unfussy as possible. Note that no special action is required if it is desired to assemble code for one sort of processor on a machine with a different processor.

Assembler definition

IPS allows the programmer to define new words as a sequence of assembler instructions. Note that assembly takes place in keyboard mode, compilation mode is not entered. (A colon definition would result in the compiler entering compilation mode.)

CODE

The introduction to an IPS named assembly routine is the word CODE followed by a name.

NEXT

The end of an assembler sequence (routine) is indicated by the word NEXT. This returns control to the emulator, and is the usual way of finishing an IPS assembly sequence.

Note that more than one exit from an assembly sequence may be provided by the multiple use of NEXT.

```
CODE a_routine (names assembly routine)

  (first action)
  …

  (last action)

NEXT (returns control to the emulator)
```

Fig 1: General layout of CODE definition

RCODE

The IPS assemblers allow the dubious practice of multiple entries to a routine. This is possible by marking an entry point with the word HIER in a CODE routine, and following this with the word RCODE followed by the name of the new entry point.

```
CODE a_routine

  (a_routine actions)
  …

HIER (deposits address on stack for RCODE following)

  (actions common to a_routine and another_routine)

NEXT

RCODE another_routine (picks up routine address from stack)
```

Fig 2: Use of RCODE construct.

Hacking

When it is necessary to write assembly routines that will be called from other assembly routines, the assembler can be used directly. This is necessary to produce replacement interrupt routines, for example.

To provide a named address, the following technique is often used:

```
0 FELD routine_name

  (start of subroutine)
  …

RET (return from subroutine)
```

Fig 3: Naming a directly-called assembler routine.

Code deposit

An assembler mnemonic, e.g. LDA, results in the corresponding machine instruction being deposited at the location that $H points to (HERE) and in $H being incremented to point to the next free position.

Operand order

The order of specifying addresses and operation follows the usual IPS principle of:

source, destination, operand.

Most conventional (algebraic) assemblers use a different order.

Mnemonics

The IPS assemblers often use the customary mnemonics for a particular processor. Some mnemonics have been changed. Note that there is little commonality between the various IPS assemblers. Equally, there is a lack of commonality in various matters between different processors.

Structured control flow

The IPS assemblers use structuring words rather than labels and gotos. There are (usually) no explicit jump/branch mnemonics.

The control structures provided are:

a) <condition> Y? N: TH

b) <condition> Y? TH

c) BEGIN <condition> END

d) BEGIN <condition> Y? TH/AGAIN

a) provides an equivalent to an IF (JA? NEIN: DANN) construct;

b) provides an equivalent to an IF statement without an else clause;

c) provides a controlled loop equivalent to the high level ANFANG ENDE? construct;

d) provides a controlled loop equivalent to the high level ANFANG JA? DANN/NOCHMAL construct.

The <condition> options allowed are specific to each assembler.

```
<condition> Y?
  (done if condition is true)
N:
  (done if condition is not true)
TH
(always done)
```

Fig 4: Use of Y? N: TH construct

```
 <condition> Y?
   (only done if condition is true)
TH
(always done)
```

Fig 5: Use of Y? TH construct

```
BEGIN
  (repeated actions)
<condition> END
(loop only exited if condition is true)
```

Fig 6: Use of BEGIN END construct

```
BEGIN
  (start of repeated actions)
  …
<condition> Y? (loop test and exit point)
  …
  (end of repeated actions)
TH/AGAIN
(loop only exited if action is false)
```

Fig 7: Use of BEGIN Y? TH/AGAIN construct

Handling of jump addresses

As with high level control constructs, the stack is used to manipulate jump addresses.

When the word Y? is met, the compiler deposits the appropriate jump code at HERE, increments $H and the value of $H is put on the stack. $H is then incremented to leave room for an unresolved jump address, which will be provided (resolved) later to the address specified on the stack.

When the TH is met later, the Y? jump address can now be resolved. HERE is the address that is to be jumped to. TH takes the address of the jump address off the stack, and stores HERE as the address for the jump associated with the Y?.

If a N: is met, a unconditional branch is assembled, again with an unresolved address field and with the address of the jump address left on the stack. The address left by the Y? is removed and the Y? is resolved to point to the position following the N: jump.

The word BEGIN is equivalent to HERE, and simply leaves the current address on the stack. This address is used by the END as the address of its conditional jump.

MYOPIA. It is possible to break the IPS structure rules by stack manipulation. Such deviant and devious practices are both unwise and liable to lose you friends.

TH/AGAIN

Early IPS assemblers did not support the use of TH/AGAIN. If not already available, define TH/AGAIN as follows:

```
: TH/AGAIN  ({loop start} {exit address field})
  VERT      ({exit address field} {loop start})
  NEVER END (return to loop start)
            ({exit address field})
  TH        (back fill exit address for Y?)
; (TH/AGAIN)
```

Fig 8: Definition of TH/AGAIN

This definition is processor independent, and relies on the handling of the jump addresses described above.

Use of regular IPS words

Because the assembler functions in interpretative mode any valid IPS words can be used in between assembly mnemonics, for instance to manipulate addresses.

The exit word NEXT can be used as often as necessary to create multiple exit points from a code word.

Assembler macros

A frequently required sequence of mnemonics etc. may be made a normal IPS definition. Each time the definition is invoked the sequence is run through again as if each mnemonic etc. had been entered individually. Such macros can contain low level structuring: Y? N: TH, BEGIN END. Because the high level IPS structure words are different from those used by the assemblers, it is possible to use conditional assembly within a macro.

IPS assembler interface

Mostly, the interface between CODE definitions and IPS is via the parameter stack. At assembler level stack operations are explicit rather than automatically managed.

6502

The stack is maintained by a pointer and appropriate machine-code instructions. If the processor already has stack-operation instructions these are usually used for the parameter stack, with the return stack simulated by a software pointer. In the case of the 6502 the machine stack is used for the return stack, with a software pointer for the parameter stack.

Before any assembly programmer is let loose at an IPS system, IPS has already taken certain machine resources into use. Particularly, certain registers and memory areas will be used for specific purposes.

The conventions should be followed, or unpredictable consequences are likely to follow.

This information can be found from

1. the relevant IPS assembler manual, and

2. the implementation notes for the particular IPS version in use.

Machine Resources

IPS requires various machine resources to run on a particular computer. Sometimes IPS' requirements can be met by existing operating system provision, often it is necessary to bypass the host's provided operating system.

Stack and memory layout

Clearly, there are two ways that can be chosen of representing a 16-bit number on a byte oriented machine:

i) Reversed address in which the least significant byte is held in the lowest address of a byte pair.

ii) High-to-low address in which the most significant byte is held in the lowest address of a byte pair.

This is one option too many for safety!

Stack layout

The stack(s) always grow from high memory to low memory. The stack normally uses the memory convention native to the processor in use.

Code and data memory layout

IPS compiled code and data grows from low memory towards high memory. IPS is designed to use the reversed address convention. In the case of those implementations which do not (6800) special conventions are necessary to allow for this.

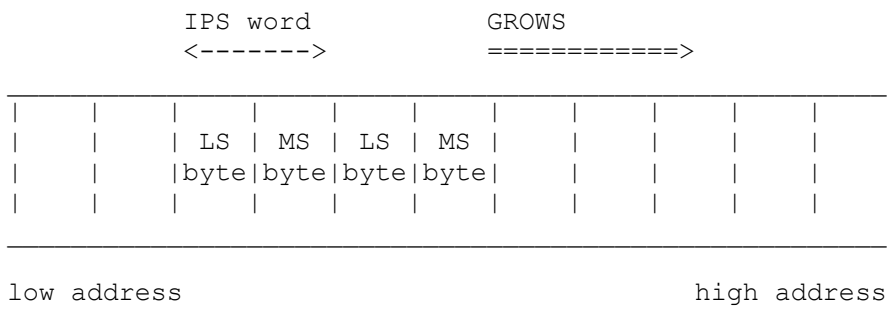
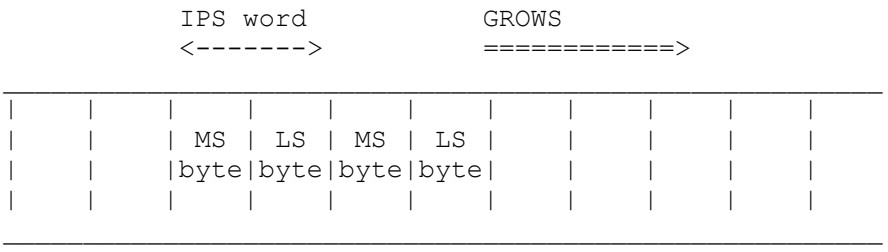


Fig 9: IPS code and data memory layout



N.B. high to low address convention.

Fig 10: IPS code and data memory layout (6800/68000)

Memory map

The memory maps of various IPS implementations vary, but tend to have a similar pattern, as typified below:

```
#FFFF     -|   Native operating system
           |
           |
           |   Hardware ports
#CFFF     -|   x    Start of parameter stack
           |   x
           |  \x/   parameter stack grows
           |
          -|
           |   |^    code grows
           |   |
           |   |
#5FFF     -|   ||   original IPS end
           |   ||
           |   ||   (compiled IPS code)
           |   ||
#400      -|   ||   start of IPS code
           |
           |        buffers etc.
           |
#200      -|
           |
           |        return stack (depth = 128 entries)
           |
#100      -|
           |
           |        emulator, etc
           |
#80       -|
           |
           |        operating system variables
           |
#00       -|
```

Fig 11: Typical IPS Memory Map

The memory map above is loosely based on the ATARI 6502 IPS implementation.

Note that the size of parameter stack is constrained by IPS code size.

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